SUPPLEMENT TO:

2640B OPTION E15

HI SPEED DISPLAY TERMINAL

MANUAL IDENTIFICATION

Manual Part No. 02640-90110

SUPPLEMENT DESCRIPTION

Option E15

This manual supplement covers the modifications to the standard HP 2640B to provide high speed operation when directly connected to a computer system. The standard data communication circuits are replaced with a high speed 8 bit parallel interface assembly. The standard 2640B diagnostics are not compatible with this modification. A self test is provided however which verifies the operation of the hi speed interface with the exception of the interface line drivers.

The HP 2640B Opt. E15 always operates in a full duplex mode and does not have any of the editing, formating or block mode capability normal to the HP 2640B. As such, the operation is greatly simplified.

The operators manual normally supplied with the 2640B is not applicable to this terminal.

The following parts and assemblies are added or deleted from the standard 2640B to make the 2640B Opt. E15.

ITEM	DESCRIPTION	PART NUMBER	QTY.
1	Keyboard, General Purpose	02640-60030	-1
2	Keyboard, Simplified	02649-60002	+1
3	Assembly, Data Com	02640-60086	-1
4	Assembly, HS Parallel Port	02640-60146	+1
5	Assembly, Control Store	02640-60144	+1
6	I.C. ROM	1818-0271	+1
7	I.C. ROM, MOS	1818-0259	-1
8	I.C. ROM, MOS	1818-0173	-1
9	I.C. ROM, MOS	1818-0174	-1
10	I.C. ROM, MOS	1818-0175	-1
11	Manual, Owners	02640-90109	-1
12	Manual, Supplement	02640-92101	+1

SUPPLEMENT

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HEWLETT hp PACKARD

DATA TERMINALS DIVISION

PREFACE

This manual supplement is intended to be used with the Service manual for the 2640B Interactive Display Terminal (02640-90015). This supplement describes the differences between the standard 2640B and the 2640B Option E15.

The 2640B Option E15 Hi Speed Data Terminal is specifically designed to provide fast data transfer between a local computer and the display in order to minimize operator wait for normal communication protocol.

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SECTION I

INSTALLATION

1-1 INTRODUCTION

This section contains the difference between the normal installation procedures and those for the HP 2640B Option E15. Unless otherwise specified, all installation procedures for the HP 2640B are applicable to the HP Option E15. There are no physical differences between the HP 2640B and the HP 2640B Option E15 with the exception of a simple keyboard arrangement and a different data communications assembly.

1-2 ACCESSORIES APPLICABLE

Due to the functional difference in intended usage and dedicated design, the HP 2640B Option E15 does not fully support all normal accessories available for the HP 2640A. Only those items listed in Table 1-1 are functional with the HP 2640B Option E15.

TABLE 1-1 APPLICABLE ACCESSORIES

PRODUCT NUMBER	FUNCTION
HP 13231A	Display Enhancement
HP 13231A Option 201	Math Character Set
HP 13231A Option 202	Line Drawing Character Set
HP 13234A	4K Memory Module
HP 13240A	Option Slot Extender
HP 13245A	Prom Character Set Kit

Refer to the applicable section of the HP 2640B Service manual for a further description and installation procedures for these accessories.

1-3 OPTIONAL OPERATING FUNCTIONS

The standard 2640B uses a number of switches on the Keyboard Interface (02640-60123) to select optional operating modes. These are not available in the Option E15. There are only two optional functions which may be selected on the keyboard interface.

1-3a UPPER CASE LOCK

Normally the HP 2640B Option E15 transmits only the 64 upper case ASCII characters to the computer interface plus the normal ASCII codes available on the keyboard. The full set of 128 ASCII characters (including the lower case alphabetic) may be transmitted to the computer interface by opening switch A on the keyboard interface PCA.

1-3b ECHO MODE

The 2640B Option E15 operates at all times in full duplex mode with independent data and control lines for transmit and receive data. The ECHO MODE option provides a display of each character as it is transmitted to the computer. Normal operation (switch B closed) requires a computer echo of the transmitted character. With the switch open the ECHO MODE option is enabled.

1-4 INTERFACE CONNECTION

1-5 GENERAL

Communications with a computer are accomplished in the 2640B Option E15 over dual 8 bit parallel data lines and with separate data transfer request and acknowledge lines (handshake). Connection to the 2640B Option E15 is through a two row 15 pin PC edge connector.

1-6 CONNECTOR INFORMATION

The mating connector to the HP 2640B Option E15 is HP part number 1251-0159 (Cinch 251-15-30-261) or equivalent. A molded plastic hood is used to protect the mating connector cable and connections. Table 1-2 provides the pin connections and signal names used. (see page 3).

TABLE 1-2 INTERFACE CONNECTIONS

PIN	SIGNAL	PIN	SIGNAL
A	$\overline{\text{DATA IN 0}}$	1	GROUND
B	$\overline{\text{DATA IN 1}}$	2	GROUND
C	$\overline{\text{DATA IN 2}}$	3	GROUND
D	$\overline{\text{DATA IN 3}}$	4	GROUND
E	$\overline{\text{DATA IN 4}}$	5	GROUND
F	$\overline{\text{DATA IN 5}}$	6	GROUND
H	$\overline{\text{DATA IN 6}}$	7	GROUND
J	$\overline{\text{DATA IN 7}}$	8	$\overline{\text{DATA OUT 0}}$
K	GROUND	9	$\overline{\text{DATA OUT 1}}$
L	$\overline{\text{DATA IN ACKNOWLEDGE}}$	10	$\overline{\text{DATA OUT 2}}$
M	$\overline{\text{DATA IN REQUEST}}$	11	$\overline{\text{DATA OUT 3}}$
N	GROUND	12	$\overline{\text{DATA OUT 4}}$
P	$\overline{\text{DATA OUT ACKNOWLEDGE}}$	13	$\overline{\text{DATA OUT 5}}$
R	$\overline{\text{DATA OUT REQUEST}}$	14	$\overline{\text{DATA OUT 6}}$
S	GROUND	15	$\overline{\text{DATA OUT 7}}$

1-7 LOGIC LEVELS AND TIMING

All signals are TTL logic compatible with ground true logic assertion. Data sent to the 2640B Option E15 must be valid on the leading edge of the Data Input Request ($\overline{\text{DIR}}$) signal and must remain valid until the leading edge of the Data Input Acknowledge ($\overline{\text{DIA}}$) signal is sent by the terminal. Data to be transmitted to the computer will be placed on the data lines and will be maintained until the receipt of the Data Output Acknowledge ($\overline{\text{DOA}}$) signal from the computer. The Data Output Request ($\overline{\text{DOR}}$) signal will be sent to the computer a minimum of 0.4 microseconds after the data lines are set.

1-10 OPTIONAL COMMUNICATIONS FUNCTIONS

1-11 GENERAL

A number of jumper locations are provided on the H.S. Parallel Port PCA part number 02640-60146 to select different modes of communications

SECTION II

FUNCTIONAL OPERATION

2-1 INTRODUCTION

This section contains the operating difference between the standard 2640B and the HP 2640B Option E15. Referenced in this section is a Functional Block Diagram of the H.S. Parallel Port card as well as a detailed Logic Diagram.

2-2 H.S. PARALLEL PORT

The H.S. Parallel Port provides high speed 8 bit parallel data communication between a computer and the display memory of the HP 2640B. All output to the HP 2640B is placed directly in the display memory without and processing by the microprocessor. The H.S. Parallel Port PCA is essentially a direct Memory Access for data input.

2-3 BUS CONTROLLER

This block is responsible for controlling the transfer of data from an external computer into the terminal RAM memory and the interaction with the terminal bus.

U11, U12, and U13 form a state machine which is synchronized to the terminal clock. U11 is a multiplexor which selects the inputs of interest in any particular state. U12 is a counter which contains the present state of the controller. U13 is a decoder which provides the control signals based upon the present state of the state machine. If a home up code (313) is present, the bus controller resets the address

2-3 BUS CONTROLLER (Continued)

The bus controller waits for the PRIOR IN and $\overline{\text{BUSY}}$ signals to be high, indicating that no other module is currently using the terminal bus. This causes the bus controller to change state from 1 to 2.

In state 2 U19 Pin 7, the EXTRA/$\overline{\text{EOP}}$ flip-flop, is set, which will indicate to the bus controller in state 7 that an extra data transfer is required to store an EOP code (316). Also, $\overline{\text{BUSY}}$ is held low to prevent other devices on the terminal bus from requesting control of the bus. If either a home up code (313) or backspace code (312) is present in the data path and handshake section as indicated by the HU+BS signal, the bus controller changes to state 3; otherwise state 4 is entered.

In state 3, U19 Pin 7 is reset to indicate that only one transfer to memory is required for the code present in the data path and handshake block. Also, DRIVE enables U54-U57, allowing $\overline{\text{BUSO-7}}$ AND ADDRO-15 to be active on the terminal bus. WRITE is held low to indicate that a write (to memory) will occur. If $\overline{\text{HOME UP}}$ is low, then RST ADDR will be low, causing the counters in the address control block to preset; otherwise $\overline{\text{INC ADDR}}$ is low, causing the counter in the address control block to increment by 1. Control is then transferred to state 4.

State 4 enables U54-U57 in the same manner as state 3. However, U19 pin 7 is not reset. Control is passed to state 5.

In state 5, $\overline{\text{REQ}}$ is brought low to strobe the data $\overline{\text{BUSO-7}}$ into the terminal memory. The bus controller remains in state 5 until $\overline{\text{WAIT}}$ goes high, indicating that the memory has received the data. At this point, the state changes to state 6.

State 6 asserts the same signals as state 5. However, control passes immediately from state 6 to state 7.

In state 7, $\overline{\text{REQ}}$ is allowed to go high. If U19 pin 7 is set, then an EOP code must be written to memory and control transfers to state 8; otherwise, control is returned to state 0.

In state 8, U19 pin 7 is reset so that only the EOP code will be stored in memory. Also, $\overline{\text{DEC ADDR}}$ is low, causing the counters in the address control block to decrement by 1 (pointing to the next lower memory location). U54-U57 are not enabled in this state. Control is immediately transferred to state 4. Control passes through states 4, 5, 6, and 7. When state 7 is reached, since state 8 has reset U19, pin 7, control goes to state 0.

2-4 ADDRESS CONTROL

This block allows the bus controller to access the RAM memory location into which the next data byte is to be stored.

U44-U47 are 4-bit presetable up/down counters configured to form one 16-bit counter, with U-47 pin 7 as the most significant bit and U44 pin 3 as the least significant bit. U44-U47 will be referred to as the "address counter" in the following discussion.

The address counter is preset if one of three conditions occur:

1. When the $\overline{\text{PON}}$ signal from the bus controller is low.

2. When the $\overline{\text{RST ADDR}}$ signal from the bus controller is low, indicating the presence of a home up code.

3. When the address counter attempts to increment past a value of 177777 octal.

The value that is preset into the address counter is (PG7) (PG6) (PG5) (PG4) (PG3) (PG2) (PG1) (PG0) 11111111 binary, where PG0-PG7 are straps inserted in U17 and the inverted values indicate that the straps are removed.

The address counter is incremented by 1 if the $\overline{\text{INC ADDR}}$ signal from the bus controller is low. Similarly, the address counter is decremented by 1 if the $\overline{\text{DEC ADDR}}$ signal is low.

To allow for both 16K and 65K memory address spaces, U68 is used as a programmable inverter; when the MSBI strap is out, U68 pin 8 is inverted from U47 pin 7 and U68 pin 6 is inverted from U47 pin 6.

The DRIVE signal from the bus controller enables U54-U57 allowing the value in the address counter to be presented on $\overline{\text{ADDR0-15}}$. If DRIVE is low, the outputs of U54-U57 are in a high impedence state.

2-5 INTERRUPT LOGIC

This logic recognizes the presence of an EOP code (316) in the data path and handshake block and optionally indicates this fact to the terminal processor.

When the REOP signal from the data path and handshake block is high, U31, pin 6 goes low. If the INT strap is in, then the $\overline{\text{ATN}}$ line is pulled low, indicating an interrupt condition to the terminal processor. Similarly, if the INT2 strap is in, then the $\overline{\text{ATN2}}$ line is pulled low, indicating an interrupt condition. The interrupt condition is cleared only when a different code replaces the EOP code in the data path and handshake block.

2-5 INTERRUPT LOGIC (Continued)

If REOP is high and $\overline{\text{REQ}}$, $\overline{\text{I/O}}$, $\overline{\text{WRITE}}$ and $\overline{\text{POLL}}$ are all pulled low by the terminal processor (to determine the source of an interrupt) then U31 pin 3 goes low and $\overline{\text{BUSO-6}}$ are pulled low if straps PLO-6 are in, respectively; only one of these straps should be inserted at any time.

2-6 DATA PATH AND HANDSHAKE

This block is responsible for routing data between the external CPU, the terminal processor, and the display memory. Logic is provided to perform a bi-directional two wire handshake between the external CPU and the PCA. Finally, a self-test facility is provided to form a data path between the terminal processor and the display memory through the PCA.

This block is divided for purposes of description into DATA PATH, HANDSHAKE WITHOUT TEST and HANDSHAKE WITH TEST portions.

2-7 DATA PATH

Output from the terminal processor on signals $\overline{\text{BUSO-7}}$ is clocked into U58 and U59 by the LATCH DATA signal from the handshake portion. This data is presented continuously to the external CPU on the output lines $\overline{\text{DOUTO-7}}$ connected to U410 and U510.

The data sent from the external CPU to the terminal on line $\overline{\text{DINO-7}}$ is inverted by U210 and U310 to provide high true signals to multiplexors U48 and U49. If the TEST signal is high, then DO-7 are selected (data from the terminal processor); otherwise, DINO-7 are selected (data from the external CPU).

At this point, LO-7 are examined by a comparator composed of U69, U51, and U38. If the code represented by LO-7 is a carriage return (15 octa then the signal CR is high (U28 pin 8). If the code represented by LO- is a line feed (12 octal), then the signal LF is high (U28 pin 12). If LF is high, L7, L6, L2 and L1 will be inverted by U39. This causes the input to U26 and U27 to change from a line feed (12 octal) to an EOL code (314 octal). If the CRLF strap is inserted, then the CR and LF signals remain low and no conversion takes place.

LO, M1-2, L3-5, M6-7 are clocked into U26 and U27 by the handshake portion. U18, U310 pin 6 and U25 form a comparator. If the code in the flip-flops U26 and U27 is a home up code (313) then the signal HOME UP (U25 pin 4 is low). If the code is backspace (312) then U25 pin 3 will be low. If either a home up or backspace code is

2-8 HANDSHAKE WITHOUT TEST

The following presentation assumes that U19 pin 4 is high i.e. TEST is false (low).

2-9 TRANSFER OF DATA FROM TERMINAL PROCESSOR TO EXTERNAL CPU

When $\overline{\text{ADDR4,9}}$ are high and $\overline{\text{ADDR10-11}}$, $\overline{\text{REQ}}$, $\overline{\text{I/O}}$ are low, this module is selected by the terminal processor. The processor must first determine if a previous transfer from processor to CPU is still being processed by performing a status request; leaving WRITE and $\overline{\text{ADDR5}}$ high and pulling $\overline{\text{ADDR6}}$ while selecting this module causes decoder U43 pin 10 to go low and U31 pin 9 to go high. If either DORI (U28 pin 4) or U310 pin 8 are high, then $\overline{\text{BUSO}}$ (U31 pin 8) will be low, indicating that a previous output handshake has not been completed. Now, if the processor holds $\overline{\text{ADDR5-6}}$ and $\overline{\text{WRITE}}$ low while selecting this module, U43 pin 15 is low, LATCH DATA (U33 pin 12) goes high, clocking processor data into U58 and U59, and a low pulse of one state time appears at U51 pin 11 after $\overline{\text{REQ}}$ goes high. This pulse causes U19 pin 9 to go low, and since TEST is low, $\overline{\text{DOR}}$ (U610 pin 3) goes low, initiating the handshake. When $\overline{\text{DOA}}$ goes low, U28 pin 2 goes low, causing U19 pin 9 to go high. U28 pin 4 goes low and U610 pin 3 goes low, completing the handshake.

2-10 TRANSFER OF DATA FROM EXTERNAL CPU TO THE DISPLAY MEMORY

When $\overline{\text{DIR}}$ goes low, the handshake is initiated. U310 pin 12 goes high and 4 state-times later (800 nanoseconds) U41 pin 3 goes high. Since U19 pin 4 is high, U29 pin 11 goes low, U29 pin 6 goes high and the handshake does not proceed further until the NEW DATA OK signal from the bus controller goes high. When this occurs, U29 pin 8 goes low, causing U28 pin 10 to go high, clocking the data into U26 and U27. When U28 pin 10 goes high, U52 and U51 generate a low-level pulse for one state time at U51 pin 3 causing DATA RDY to go high to the bus controller if CR is low (i.e. the bus controller does not process carriage return codes). Also, a half state-time pulse at U42 pin 8 causes U19 pin 9 to go high. Finally, U19 pin 13 goes high, causing $\overline{\text{DIA}}$ (U610 pin 6) to go low to acknowledge the receipt of the data to the external CPU. When $\overline{\text{DIR}}$ returns to a high state, U41 pin 3 immediately goes low causing U29 pin 11 to go high and U29 pin 6 to go low. This causes U19 pin 13 to go low, $\overline{\text{DIA}}$ (U610 pin 6) goes high and the handshake is completed.

2-11 ENTERING THE SELF-TEST MODE

When this module is selected and $\overline{\text{ADDR6}}$ and $\overline{\text{WRITE}}$ are high and $\overline{\text{ADDR5}}$ is low, then U43 pin 9 goes low and U19 pin 4 goes low, causing the TEST signal (U28 pin 6) to go high.

2-12 HANDSHAKE WITH TEST

The following presentation assumes that U19 pin 4 is low. i.e. TEST is true (high).

2-13 TRANSFER OF DATA FROM THE TERMINAL PROCESSOR TO THE DISPLAY MEMORY

When the processor drives the bus signals so that U43 pin 15 goes low, LATCH DATA (U33 pin 12) goes high and DORI (U28 pin 4) goes high (see the analysis in section 2-8 for transfer from processor to CPU). Since TEST is high, DOR does not change its level (no handshake with the external CPU occurs) and U29 pin 3 goes low, and U29 pin 6 goes high. When NEW DATA OK goes high, U29 pin 8 goes low, U28 pin 10 goes high, clocking U26 and U27 and initiating a one state-time pulse on U51 pin 3. This low pulse will cause DATA RDY to go high if CR is low and the half state-time pulse generated at U42 pin 8 will cause U19 pin 9 to go high and DORI to go low. Then U29 pin 3 goes high, U29 pin 6 goes low, U29 pin 8 goes high and the internal handshake is completed. Since TEST is high, U29 pin 11 and DIA (U610 pin 6) are forced high, inhibiting any handshake with the external CPU.

2-14 LEAVING THE SELF TEST MODE

When this module is selected and WRITE and ADDR5-6 are high then U43 pin 7 goes low and U19 pin 4 goes high, causing the TEST signal (U28 pin 6) to go low.

SECTION III

SERVICE

3-1 INTRODUCTION

This section contains the differences and unique service procedures for the HP 2640B Option E15. This information will allow isolation of malfunctions to a replaceable assembly.

3-2 TROUBLESHOOTING

3-3 APPLICABLE PROCEDURES

The standard troubleshooting procedure for the HP 2640B as outlined in the Service Manual are applicable to the HP 2640B Option E15 with the following exceptions.

Paragraph	Procedure
3-5	Keyboard and Communications Group Checkout
3-6a	Delete reference to transmit indicator
3-6b	Delete reference to cursor (delete paragraph)
3-6c (1)	Delete reference to indicator lights (delete paragraph)
3-6c (6)	Delete reference to cursor

3-4 TROUBLESHOOTING CHART

Figure 3-1 of the HP 2640B Service Manual is applicable to troubleshooting of the HP 2640B Option E15 with the following exceptions:

3-4 (a) CURSOR - The HP 2640B Option E15 does not have the cursor circuits enabled, as such all reference to the cursor must be ignored.

3-4 (b) INDICATORS - The HP 2640B Option E15 does not have indicators on the keyboard. Delete all references to such indicators.

3-4 (c) DATA COMM - The data comm assembly has been replaced by the H.S. Parallel Port.

3-5 SELF TEST

The HP 2640B Option E15 incorporates a comprehensive self test feature which will verify all terminal operation including the H.S. Parallel Port I/O PCA with the exception of the data communication line drivers and receivers. The only major component not verified by the self test is the keyboard.

SECTION IV

REPAIR

4-1 INTRODUCTION

This section describes the changes to the standard HP 2640B Repair section and provides a list of parts for the unique assemblies in the HP 2640B Option E15.

4-2 PARTS LIST

Table 4-1 indicates changes to be made to Table 4-1 of the standard HP 2640B Service Manual.

TABLE 4-1

FIG & INDEX #	HP PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
047	1818-0173	I.C. ROM, MOS	-1
	1818-0174	I.C. ROM, MOS	-1
	1818-0175	I.C. ROM, MOS	-1
	1818-0259	I.C. ROM, MOS	-1
	1818-0271	I.C. ROM, MOS	+1
050	02640-60086	ASYNCHRONOUS DATA COMM. ASSEMBLY	-1
	02640-60146	H.S. PARALLEL PORT ASSEMBLY	+1
	02640-60180	KEYBOARD ASSY.	-1
	02649-60002	SIMPLIFIED KYBD.	+1
	5061-1340	CONNECTOR KIT	+1
047	02640-60144	G.P. BASIC MEMORY ASSY.	+1

TABLE 4-2

H.S. PARALLEL PORT PARTS LIST

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.	QTY.
C2-20	Cap .01 µf	0160-2055	19
C1	Cap 39µf 10V	0180-0393	1
TP1	Stud Solder Term	0360-0124	1
R5	Res 100 5% .25	0683-1015	1
R7, 8	Res 220 5% .25	0683-2215	2
R4, 6	Res 4700 5% .25	0683-4725	2
XA16	Socket 8 Dip Lo	1200-2455	1
XA14, 15, 17	Socket 16 Dip Lo	1200-0482	3
U110	Network Res Dip	1810-0081	1
R3	Res Net 8X1K	1810-0121	1
R3	Res Net 8X200	1810-0163	1
R1	Network Res Dip	1810-0164	1
U61	IC SN74LS02N	1820-1144	1
U44-47	IC SN74LS193N	1820-1194	4
U26, 27 U52, 58, 59	IC SN74LS175N	1820-1195	5
U34	IC SN74LS174N	1820-1196	1
U22, 29 U51	IC SN74LS00N	1820-1197	3
U28, 33	IC SN74LS04N	1820-1199	2
U18, 23 U35, 41	IC SN74LS08N	1820-1201	4
U24, 32 U42	IC SN74LS32N	1820-1208	3
U21, 31 U53, 41, 510, 610	IC SN74LS38N	1820-1209	6

TABLE 4-2 (cont'd.)

H.S. PARALLEL PORT PARTS LIST

REFERENCE DESIGNATOR	DESCRIPTION	PART NUMBER	QTY.
U54-57	IC DM80 96N	1820-1368	4
U210, U310	IC SN74LS14N	1820-1416	2
U13, 25 U38	IC SN74LS42N	1820-1418	3
U12	IC SN74LS161N	1820-1430	1
U19	IC SN74LS279N	1820-1440	1
U36, 37 U48, 49	IC SN74LS157N	1820-1470	4
CR1	Diode-Silicon	1901-0050	1
	Board Etched	02640-80146	1

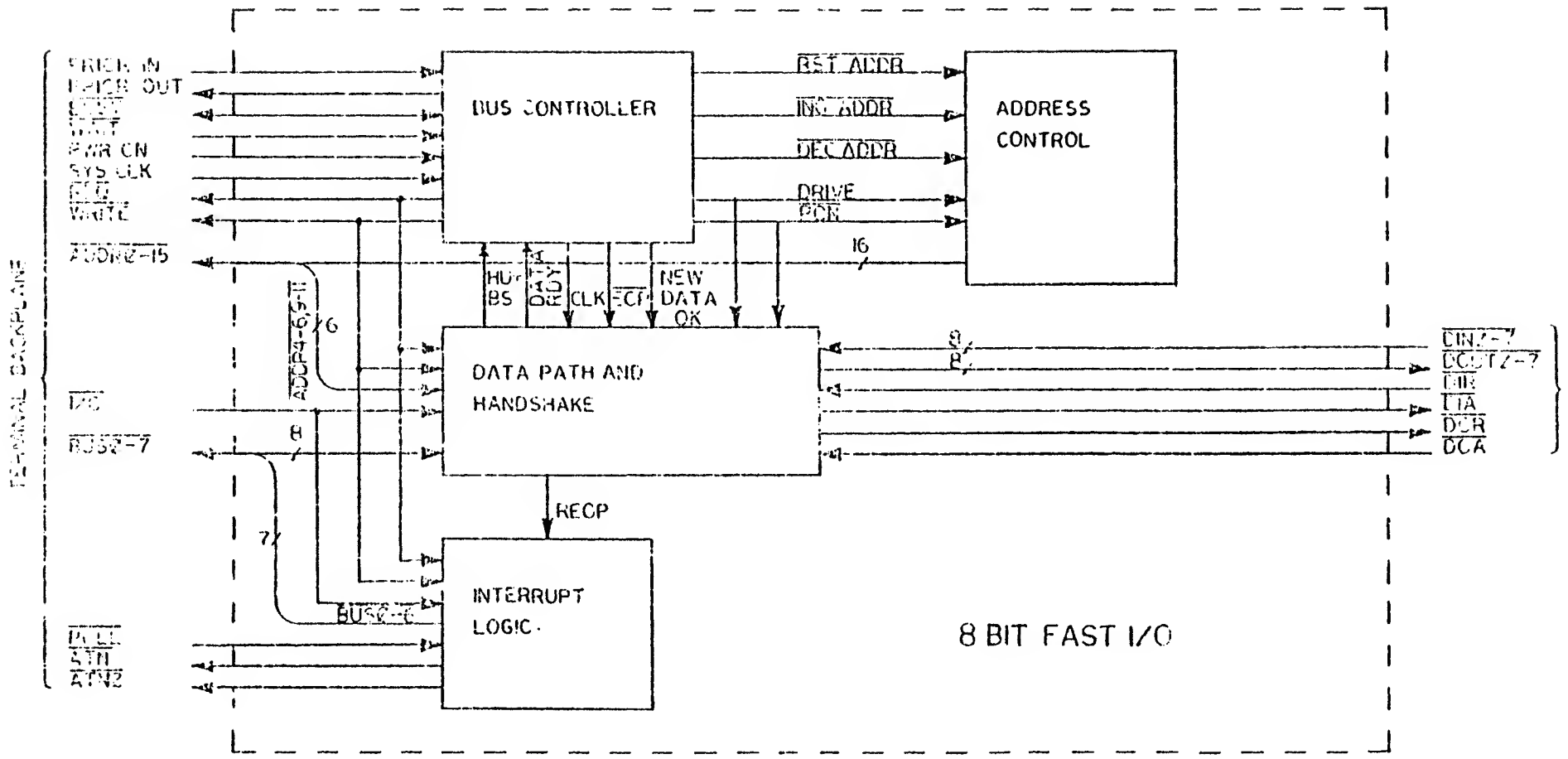

FIGURE 2-1

H.S. PARALLEL PORT

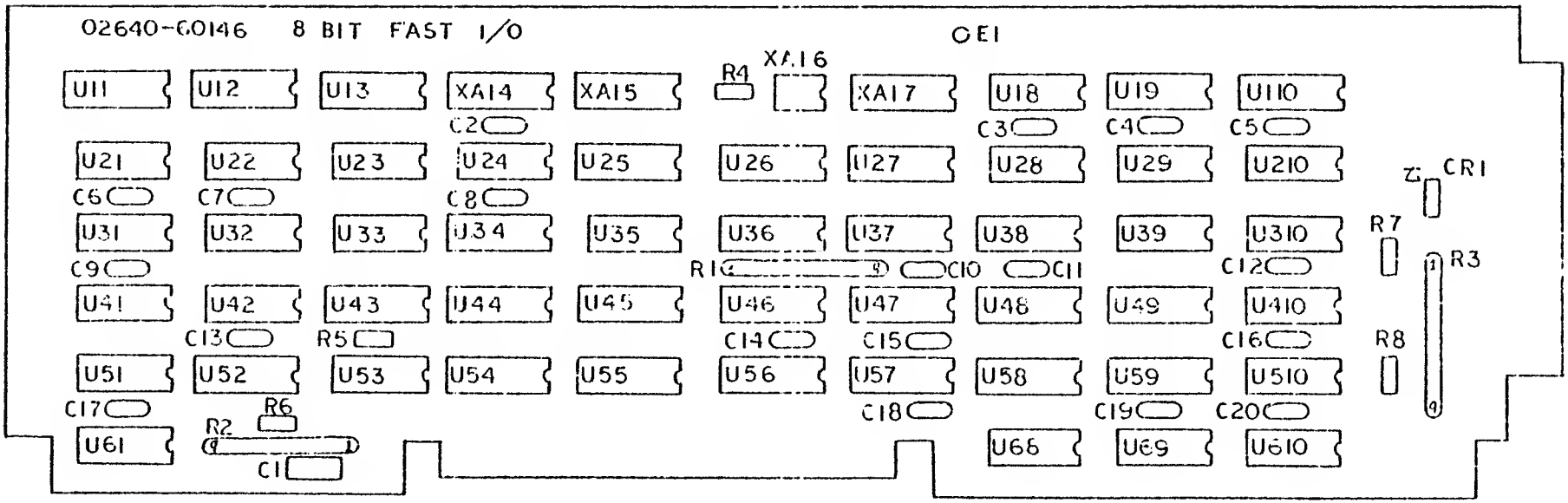

FIGURE 4-2

H.S. PARALLEL PORT
COMPONENT LOCATION